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Original Article

Using a Kogge Stone Adder to Create Low-Area-Delay Pulsed Latches for a Shift Register

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Abstract: *This work suggests a delay-efficient architecture for shift registers by replacing flip flops with pulsed latches. Using latches instead of flip flops is an excellent way to save space and power. Adding the required delays in pulses for latches helps mitigate the timing issue they display. Included in this is a delay-generating pulse counter. The delays can be obtained simply adding one to the counter. The proposed kogge stone architecture generates several deviations from the standard adder design while simultaneously minimizing delay to the greatest possible extent.*

Keywords: *Flip flops, Latches, KOGGE stone adder .Software used: Xilinx12.3* Language used: Verilog HDL.

I. INTRODUCTION

All of a chip's components have same dynamic power consumption. The clock network is a significant dynamic power user. Therefore, saving energy in the clock network can have a major effect on the total dynamic power. Multiple methods exist for designers to decrease clock power by utilizing smaller clock buffers. Clock networks can have a lot of dynamic power even using these methods, because registers are used as state elements. The register is often implemented with a flip-flop. (2) Combinational logic circuits are time independent logic circuits because their outputs can be determined by applying the logic function of the input state at any given moment. (3)Sequential logic circuits are digital logic circuits whose outputs can be decided by the logic function of current state inputs and previous state inputs. These sequential digital logic circuits can save the current inputs and the system's previous state. Therefore, the data can be stored digitally in these sequential digital logic circuits, which is not the case with combinational logic circuits. These memories are a part of the sequential logic circuits.

II. LITERATUREREVIEW

A. SRLatch:

Two NAND gates are cross-coupled to create the SR latch. Until the latch state needs to be altered, it works with both inputs set to 1. When the S input is grounded to zero, the latch is in the set state and the output Q is one. The circuit maintains its predetermined state once the S input is reset to 1. Once the L and S inputs have returned to 1, we can toggle the latch's state by setting the R input to 0. When contrasting the NAND with the NOR latch, keep in mind that the NAND's input signals need the inverse of the values used by the NOR latch.

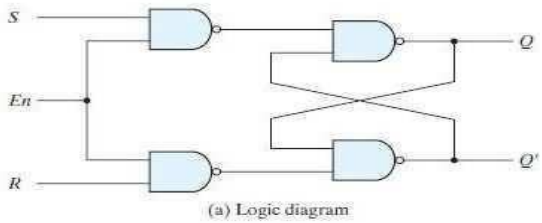

Figure1: SR-Latch

Table 1: Truth Table of SR Latch

En	S	R	Next State of Q
0	X	X	No Change
1	0	0	No Change
1	0	1	Q = 0; reset state
1	1	0	Q = 1; set state
1	1	1	Indeterminate

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B. D-Latch:

Making ensuring that inputs S and R never equal 1 at the same time is one technique to prevent the unfavorable condition of the indeterminate state in the SR latch. The D latch is where this processing takes place, and as can be seen, it accepts just D and En as inputs.

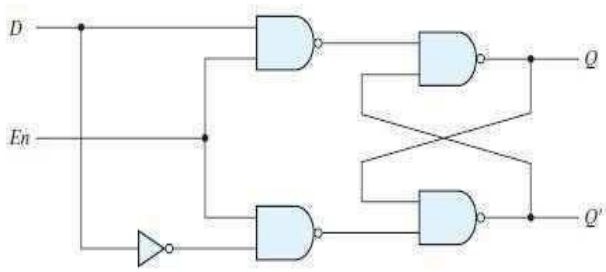

Figure 2: D-Latch

Table 2: Truth Table of D-Latch

En	S	Next State of Q
0	X	No Change
1	0	Q = 0; reset state
1	1	Q = 1; set state

C. JK-Latch:

The JK flip-flop is more commonplace than the JK latch. The following is a table of states for use with the JK latch

Table 3: Truth Table of JK-Latch

J	K	Q_{next}	Comment
0	0	Q	No Change
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}$	Toggle

To ensure correct operation in a sequential circuit sharing a common clock, flip-flop circuits are designed in such a way. The latch has a flaw in that it is sensitive to the strength of a clock pulse.

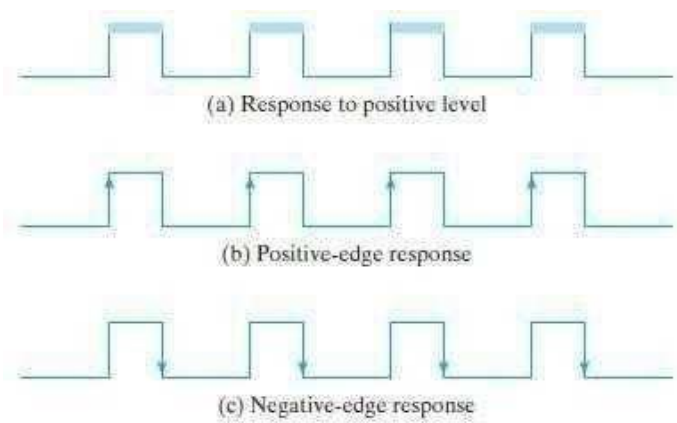

Figure 3: Positive and Negative Clock Edge Cycle

D. SR-Flip-flop:

The SR flip-flop, sometimes called an SR Latch, is one of the simplest types of sequential logic circuit. This basic flip-flop is a one-bit memory bi-stable device with two inputs, S and R, where S causes the output to be "SET" (or "1") and R causes it to be "RESET" (or "0") respectively.

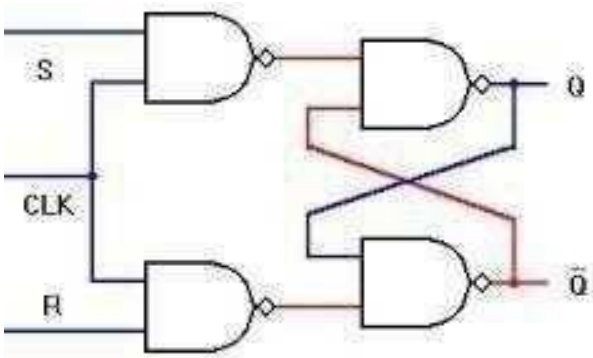

Figure 4: SR-Flip-Flop Circuit

E. D Flip-flop:

The D flip-flop has seen extensive use. Another name for this flip-flop is "data" or "delay" flip-flop. When the D-input is read, the D flip-flop stores the value of that input at a specific time in the clock cycle (often the rising edge of the clock).

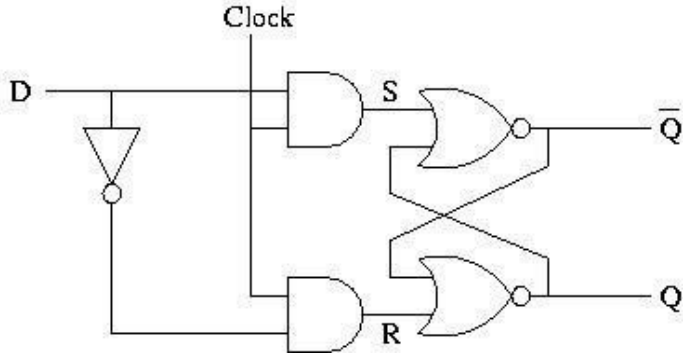

Figure 5: D-Flip-Flop

F. JK Flip-flop:

In order to avoid an illegal or invalid output state that can occur when both inputs S and R are equal to logic level "1," the JK flip flop is essentially a gated SR flip flop with additional clock input hardware. A JK flip-flop has four possible input states—logic 1, logic 0, no change, and toggle—because of the additional timed input. The symbol for a JK flip flop is similar to the one we saw in Lesson 1, with the addition of a clock input.

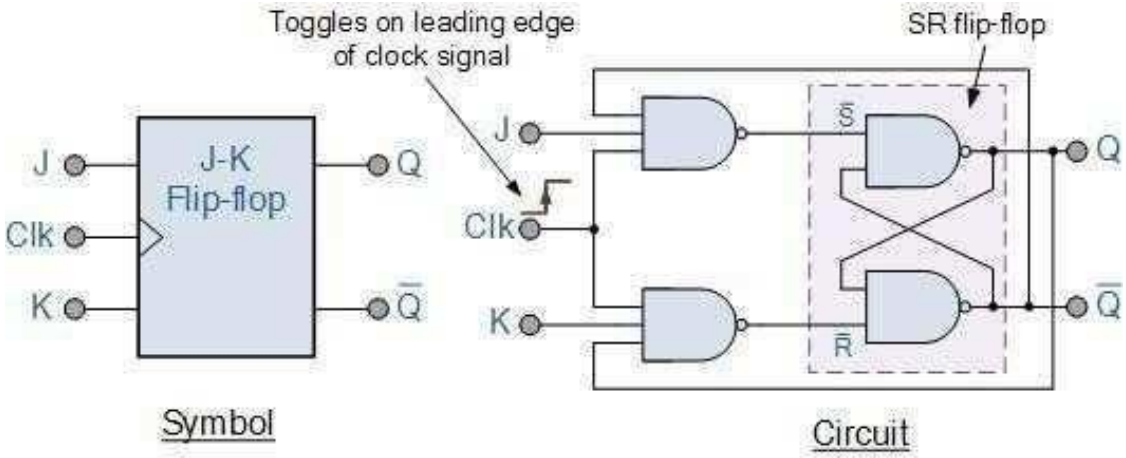

Figure 6: JK Flip-Flop Circuit and Logic Symbol

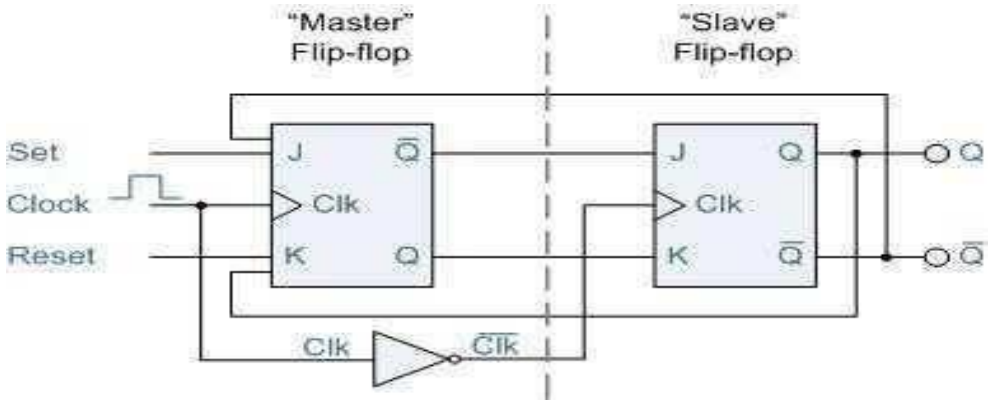

Figure 7: Master-Slave JK Flip-Flop Symbol

While the clock (Clk) input is "HIGH" at logic level "1," the input state represented by signals J and K are "locked" in the gated "master" SR flip flop. Since the clock input of the "slave" SR flip flop is the inverse (complement) of the clock input of the "master" SR flip flop, the "slave" SR flip flop does not toggle. For the slave flip flop to "see" the outputs from the master flip flop, the clock input must be at logic level 0. The "Synchronous" nature of the flip flop arises from the fact that data can only be sent when the clock signal is also present.

G. Pulse Latch:

Pulse generators, which use a source clock to produce pulse clock waveforms, are necessary for the pulsed latch. The pulse width is adjusted to make the change as smooth as possible.

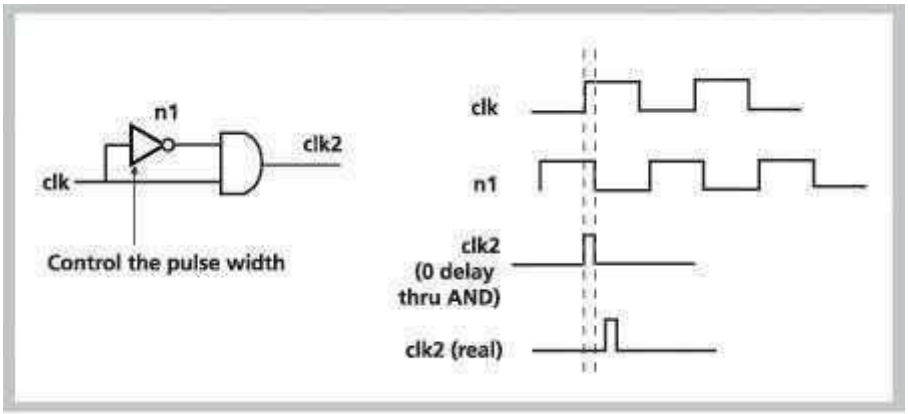

Figure 8: Pulse Latch

II. SHIFT REGISTERS AND LATCH PULSE ARCHITECTURE

Registers are built with flip-flops. A register stores information using a bank of flip flops. To hold 16 bits of information, for instance, a computer requires 16 flip flops. A register's inputs and outputs can be either serial or parallel, depending on the application. In a shift register, data is stored and moved closer to the output at the beginning of each clock cycle. There are four primary varieties of shift registers.

They are:

- Serial in serial out shift register
- Serial in parallel out shift register
- Parallel in serial out shift register
- Parallel in serial out shift register

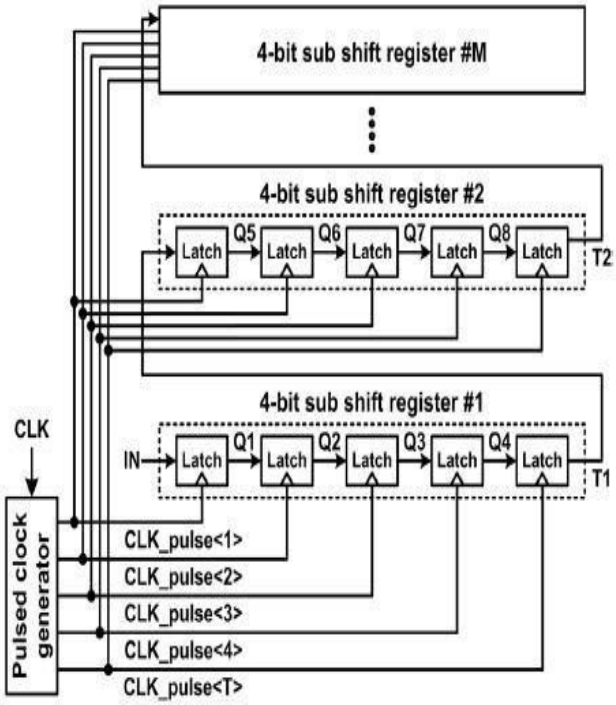

Figure 9: Pulsed Latch Architecture

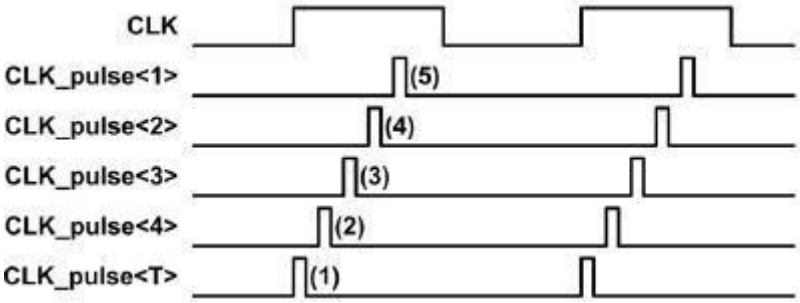

Figure 10: Clock Signals

Optimization of electricity consumption is analogous to optimization of floor space. Latch and clock-pulse circuits account for the bulk of the energy drain. Power is used to transfer data and load clocks into each latch. Power consumption for a latch and a clock-pulse circuit are 1 and, respectively, when the circuit powers are normalized with a latch. As a whole, we use a lot of energy. The smallest integer that can be divided by is chosen for this purpose. Clock buffers are ignored during the selection process. The total clock loading of latches determines the total size of the clock buffers.

The parasitic capacitance and resistance of a long wire prevent a small clock pulse from traveling through a lengthy shift register. The clock pulse shape degrades at the wire's end because the rising and falling times of the pulse lengthen as a result of the wire's delay.

III. DESIGNTOOLS

The abbreviation for "Very Large Scale Integration" is "VLSI." This is the area where increasing densities of logic devices are being packed into ever-smaller spaces.VLSI

- An integrated circuit is, in a nutshell, a collection of transistors on a single chip.
- An IC could include millions of transistors, each measuring just a few millimeters in width and length.

Widespread use: virtually all electronic logic devices

VHDL, Verilog, System verilog, etc. are just few of the languages used in VLSI technology design. The design is written in Verilog.

A. ApplicationsofVLSI:

These days, we rely on electronic technologies for pretty much everything. Mechanisms that once functioned mechanically, hydraulically, or in some other way have sometimes been replaced by electronic systems, which are typically smaller, more flexible, and easier to service. In other instances, electronic systems have given rise to wholly novel uses. Some of the functions of electronic systems are more obvious than others.

- Portable media gadgets like MP3 players and DVD players run complex algorithms while consuming surprisingly little power.
- In consumer electronics, digital electronics can compress and decompress video on the fly, even at high resolution data rates.

Despite their specialized purpose, even low-cost terminals for Web browsing require complex technology.

B. Xilinx:

Synthesis tasks are performed by VHDL/VERILOG designers using Xilinx software. FPGA allows for the synthesis and configuration of any simulated code. During synthesis, the VHDL code is converted into a gate-level net list. It is now standard practice in the design process.

C. Algorithm:

- Start the ISE Software by clicking the XILINXISE icon.
- Create New Project
- And find the following properties display
- Create a DHDL source formatting all inputs, outputs and buffers if required
- VHDL code, to be synthesized
- Check Syntax after finally editing the VHDL source for any errors.
- After that, perform the RTL and TECHNOLOGY schematic for verifying synthesis

D. Verilog Language:

In the world of integrated circuit (IC) design, Verilog hdl is one of the two most popular Hardware Description Languages (HDL). VHDL is an additional coding language. To fix faults or test with a different design, HDL allows for early replication of the design during the design cycle. Hdl architectures are independent of technology, easy to build and rectify, and typically more comprehensible than their schematic counterparts. There are typically four layers of abstraction used when describing Verilog styles.

- Algorithmic level
- Register transfer level
- Gate level
- Switch level

Erects that may be worn to limit simulation input and output are also described in the language. It appears that not all Verilog constructions are being electronically realized. Non synthesizable structures should be reserved for use on test benches only because most readers will need to physically fabricate their circuits. When referring to specific examples or constructions that cannot be synthesized, the phrase "not synthesizable" will be used. There are typically two varieties of code used in HDLs; *Structural, structural diagrams are memory-free linguistic wiring*.

p = (q) & (r); assign a=b | c & d; /* "|" is an OR */ the statements can be listed in any order you choose. If we alter c, then we can alter a.

A procedure that is used in memory-equipped circuits or the proper way to hand-write conditional logic.@(posedgeclk) // always, On each rising clock edge, run the following sentence.
For example, count = count+1;

This kind of thinking generates an unnecessary amount of memory for composites that use flip-flop memory. However, procedural code is preferred by many since it is much simpler to write. For instance, if and case statements can only be used in procedural code. This motivates the development of synthesizers that can properly recognize constrained varieties of procedural code as truly combinatory. However, tread carefully if you stray from this fashion.

The language Verilog supports four distinct modeling techniques. They represent • the modeling level of a switch.

- The modeling at the gate level.
- The Modeling of Data Flow
- Modeling of behavior

IV. RESULTS AND DISCUSSIONS

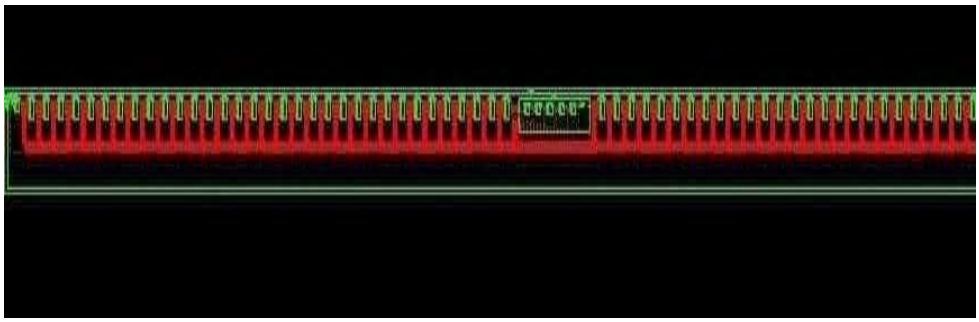

Figure 11: RTL Schematic

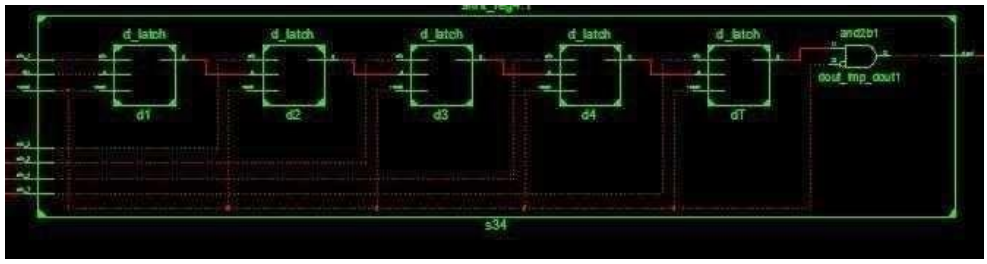

Figure 12: RTL Internal Structure

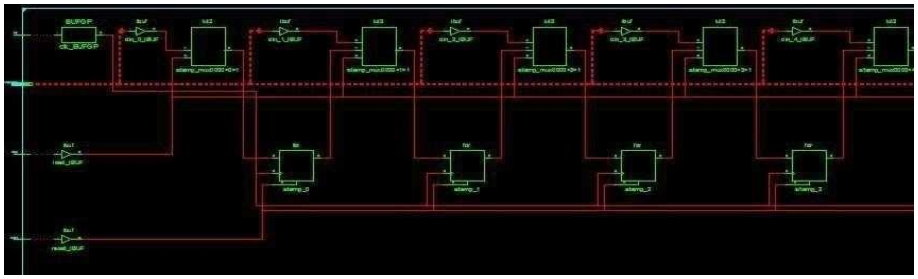

Figure 13: Technology Schematic

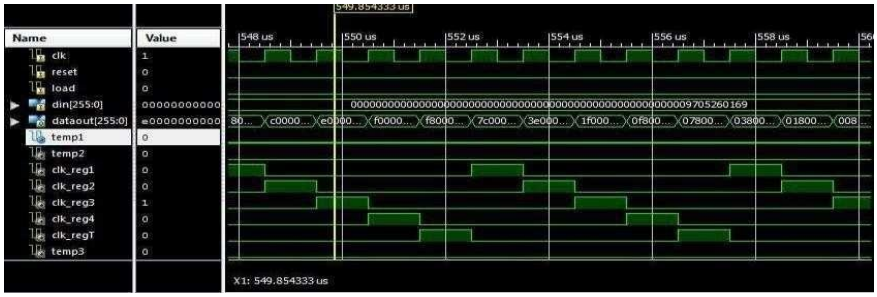

Figure 14: Simulation Results and Related Timing Diagrams

V. CONCLUSION

In this work, we suggest a shift register that makes little use of delays by making use of pulsed latches. Pulsed latches produce outcomes comparable to flip flops while using fewer physical components. The latches on a pair of flip flops. Using a timed latch with a pulse signal as the clock input yields the same outcomes. As a result, less hardware is needed, and in this project, the latches are activated by a counter design that generates several clock pulses. The circuit that does this is called a "counter," and it works by adding one to the previous number. During the boosting procedure, multiple adders are used. This work suggests using a kogge stone adder, which has a delay of 0.932 ns compared to the standard adder's delay of 3.497 ns.

VI. REFERENCES

[1] P. Reyes, P. Reviriego, J. A. Maestro, and O. Ruano, “New protection techniques against SEUs for moving average filters in a radiation environment,” IEEE Trans. Nucl. Sci., vol. 54, no. 4, pp. 957–964, Aug. 2007.

[2] M. Hatamian et al., “Design considerations for gigabit ethernet 1000 base-T twisted pair transceivers,” Proc. IEEE Custom Integr. Circuits Conf., pp. 335–342, 1998.

[3] H. Yamasaki and T. Shibata, “A real-time image-feature-extraction and vector-generation vlsi employing arrayed-shift-register architecture,” IEEE J. Solid-State Circuits, vol. 42, no. 9, pp. 2046–2053, Sep. 2007.

[4] H.-S. Kim, J.-H.Yang, S.-H.Park, S.-T.Ryu, and G.-H. Cho, “A 10-bit column-driver IC with parasitic- insensitive iterative charge-sharing based capacitor-string interpolation for mobile active-matrix LCDs,” IEEE J. Solid-State Circuits, vol. 49, no. 3, pp. 766–782, Mar. 2014.

[5] S.-H. W. Chiang and S. Kleinfelder, “Scaling and design of a 16-megapixel CMOS image sensor for electron microscopy,” in Proc. IEEE Nucl. Sci. Symp. Conf. Record (NSS/MIC), 2009, pp. 1249–1256.

[6] S. Heo, R. Krashinsky, and K. Asanovic, “Activity-sensitive flip-flop and latch selection for reduced energy,” IEEE Trans. Very Large Scale Integer. (VLSI) Syst., vol. 15, no. 9, pp. 1060– 1064, Sep. 2007.

[7] S. Naffziger and G. Hammond, “The implementation of the nextgeneration 64 b itanium microprocessor,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2002, pp. 276–504.

[8] H. Partovi et al., “Flow-through latch and edge-triggered flip-flop hybrid elements,” IEEE Int. Solid-State Circuits Conf(ISSCC) Dig. Tech. Papers, pp. 138–139, Feb. 1996.

[9] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, “Conditional push-pull pulsed latch with 726 fJops energy delay product in 65 nm CMOS,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2012, pp. 482–483.

[10] V. Stojanovic and V. Oklobdzija, “Comparative analysis of masterslave latches and flip-flops for high- performance and low-power systems,” IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[11] J. Montanaro et al., “A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor,” IEEE J. Solid-State Circuits, vol. 31, no. 11, pp. 1703–1714, Nov. 1996.

[12] S. Nomura et al., “A 9.7 mW AAC-decoding, 620 mW H.264 720p 60fps decoding, 8-core media processor with embedded forwardbody-biasing and power-gating circuit in 65 nm CMOS technology,” in IEEE Int. Solid- State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2008, pp. 262–264.

[13] Y. Ueda et al., “6.33 mW MPEG audio decoding on a multimedia processor,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2006, pp. 1636–1637.

[14] B.-S. Kong, S.-S.Kim, and Y.-H. Jun, “Conditional-capture flip-flop for statistical power reduction,” IEEE J. Solid-State Circuits, vol. 36, pp. 1263–1271, Aug. 2001.