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Original Article

Effective Error Detection in VLSI Circuits Using Comparators

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Abstract: *This study focuses on providing simulation results and analysis of a fault-tolerant voter circuit, with a specific emphasis on the Triple Modular Redundant (TMR) system. TMR systems enhance the robustness of the voter circuit by introducing redundancy at the logic level. The proposed technique aims to minimize the area cost while ensuring multiple fault detection capability. To achieve this, a novel voter circuit has been developed and implemented using Verilog HDL. The circuit's performance has been thoroughly evaluated through extensive simulations using Xilinx 12.1 software. By improving the robustness of the voter circuit in a TMR system, this work contributes to enhancing the overall reliability and fault tolerance of nanoelectronic systems. The proposed voter circuit designed with minimum area cost considerations, offers efficient multiple fault detection capabilities. The use of Verilog HDL and Xilinx 12.1 simulations provides a comprehensive evaluation of the circuit's performance, ensuring its feasibility and effectiveness in practical implementations. Overall, this research work sheds light on the importance of hardware redundancy in mitigating the higher defect rates observed in nanoelectronics. By focusing on the development and evaluation of a robust voter circuit within a TMR system, this study paves the way for more reliable and fault-tolerant nanoelectronic systems, enabling them to operate seamlessly even in the presence of inherent defects and challenges.*

Keywords: *VLSI Circuit, Comparators, TMR System.*

I. INTRODUCTION

In the realm of nanoelectronics, the defect rate is significantly higher compared to conventional CMOS circuits. To address this challenge and ensure fault tolerance at the nano level, hardware redundancy has emerged as a promising solution. A vital component of a redundancy-based fault-tolerant system is the voter circuit, which enables the system to continue functioning correctly even in the presence of one or more faults within its components. The reliability of the fault-tolerant system heavily relies on the robustness of the voter circuit.

In the realm of VLSI (Very Large Scale Integration) design, ensuring the reliability and fault tolerance of electronic systems is of paramount importance. With the ever-increasing complexity and shrinking transistor sizes, the risk of errors and faults has become a significant challenge. To address this, researchers and engineers have developed various fault-tolerant techniques, one of which is Triple Modular Redundancy (TMR). In this introduction, we embark on a journey to explore the principles, advantages, and applications of TMR-based fault-tolerant systems in VLSI design.

The pursuit of fault-tolerant systems in VLSI design has been driven by the need to ensure reliable operation in the face of faults and errors. Traditional fault tolerance techniques often involve redundancy in the form of replicated circuitry or error detection and correction codes. However, Triple Modular Redundancy presents a robust approach that leverages the concept of majority voting to detect and recover from faults with high reliability.

Triple Modular Redundancy is a fault-tolerant technique that employs triplicate modules to achieve fault detection and correction. In a TMR-based system, three identical modules are used to perform the same computation or task simultaneously. The outputs of these modules are then compared, and a majority vote is taken to determine the correct output. By utilizing a voting mechanism, TMR can effectively detect and correct errors, thereby ensuring the system's overall reliability.

The key advantage of TMR lies in its ability to mitigate transient faults, which are temporary errors caused by various factors such as radiation, electromagnetic interference, or voltage fluctuations. Due to the triplicate nature of the modules, any transient fault occurring in one module can be detected and overridden by the majority vote, ensuring correct operation. This fault tolerance capability makes TMR particularly valuable in safety-critical applications where system failures can have severe consequences.

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II. SURVEY

Luis et al present an approach to address issues encountered when using commercial EDA tools for designing fault-tolerant circuits based on the Triple Modular Redundancy (TMR) technique. The optimization process performed by these tools often removes the added redundant logic or imposes additional constraints that result in suboptimal fault-tolerant designs. To overcome this, the authors propose an automated approach for implementing, optimizing, and verifying TMR circuits in commercial technologies.

Pan Zheng et al focus on analyzing the problem of Signal Integrity in the design of high-speed communication between modules of a Triple Modular Redundant (TMR) computer. Specifically, they investigate the detrimental effects caused by Reflection and Simultaneous Switching Noise (SSN) and propose solutions to improve the design. Through simulations and verification tests with the complete computer system, the authors validate the effectiveness of their proposed design enhancements, which encompass layout improvements, circuit design modifications, and signal link optimization.

Shengyang Mao et al introduce a novel methodology called Optimal Partitioning Triple Modular Redundancy (OPTMR) to optimize the Data Flow Graph (DFG) partitioning process in TMR circuits. The goal is to reduce the overall overhead associated with TMR implementation. The authors discuss the mathematical relationship between DFG partitioning and total overhead and present the principles of DFG node division. By applying their OPTMR methodology, the authors demonstrate the potential for significant overhead reduction in TMR systems.

Subrata et al aim to implement a novel fault-tolerant structure for the majority voter in Triple Modular Redundancy (TMR) systems using Quantum-dot Cellular Automata (QCA), a promising nanotechnology alternative to CMOS VLSI. The proposed structure leverages the unique properties of QCA to enhance fault tolerance in TMR-based systems. By utilizing QCA, the authors seek to improve the reliability and resilience of fault-tolerant circuits.

Hossein Soltani et al compare the reliability of systems employing triple and five modular redundancy. They define reliability in conditional probability terms, referring to the ability of a system to operate properly within a given timeframe, provided it was healthy at the beginning of that timeframe. The authors explore the enhancement of reliability through fault tolerance implementation in computer systems.

Yan Li et al propose a complementary dual-modular redundancy (CDMR) scheme for mitigating the effects of soft errors. Inspired by the Markov random field (MRF) theory, the authors implement a two-stage voting system in CDMR. This includes a first-stage optimal MRF structure and a second-stage high-performance merging unit. The CDMR scheme aims to improve fault tolerance and reliability by incorporating these voting stages.

Yoshizumi Ito et al introduce Triple Modular Redundancy (TMR) on parallel-operation-oriented Optically Reconfigurable Gate Arrays (ORGA). They demonstrate that ORGA supports high-speed reconfiguration and high-density parallel operations. The authors discuss the benefits of the parallel-operation-oriented ORGA design, which features multiple programmable gate array layers sharing a common configuration context to increase the number of implementable parallel operations.

Nguyen et al propose an approach for computing the reliability of TMR-MER systems that consist of a finite number of components. The authors derive reliability models and demonstrate that system reliability improves when critical components are checked more frequently for the presence of configuration memory errors. They compare this approach to round-robin checking methods and highlight its effectiveness in improving system reliability.

Rahul Parhi et al present a novel approach called partial Triple Modular Redundancy (PTMR) that achieves fault tolerance similar to or better than traditional TMR while significantly reducing hardware overhead. PTMR selectively computes only the most significant bits of the result using TMR, focusing on preserving critical information. By doing so, the authors aim to minimize hardware requirements while maintaining fault tolerance capabilities.

Ryo Terada et al propose a high-soft-error-tolerant 16-bit adder unit based on penta-modular redundancy (SMR) in addition to triple modular redundancy (TMR). The authors analyze the soft-error tolerances of TMR and SMR and conduct error-injection experiments on a field-programmable gate array (FPGA) to validate their findings. The results reveal the usefulness of SMR for mitigating errors in heavy radiation environments.

Tooba Arifeen et al investigate the vulnerability of Approximate Triple Modular Redundancy (ATMR) in the presence of critical inputs, where faults can lead to output errors. The authors employ automatic test pattern generation to identify critical input spaces and prevent approximation techniques from being applied to those modules within TMR. This ensures the reliability and accuracy of the overall system.

Minoru Watanabe et al implement a parallel-operation-oriented FPGA to efficiently handle parallel operations. This FPGA architecture features multiple programmable gate array layers sharing a common configuration context, enabling perfect removal of overlapping data in the configuration memory. By eliminating overlap, the design optimizes parallel operation implementation.

Sai Aparna Aketi et al analyze the effectiveness of GDMR (Gate Diffusion Input MOS Redundancy) against the well-known Triple Modular Redundancy (TMR) technique for handling Multiple Event Transients (METs). Through comparative experiments using unhardened, GDMR, and TMR logic gates in UMC 65nm technology, the authors demonstrate that GDMR logic gates exhibit better tolerance to METs, except for certain cases. Their findings contribute to understanding the reliability of GDMR and TMR under MET conditions.

Umar Afzaal et al propose a self-checking voting circuit for consensus voting on FPGAs, aiming to increase reliability. Through fault injection and reliability analyses, the authors demonstrate that the proposed redundant voting copies enhance reliability by approximately 26% compared to an unprotected simplex voter. Their approach ensures reliability in a wide range of applications by averaging reliability values of voters over normalized time.

III. PROPOSED SYSTEM

With the increasing prevalence of faults and defects, both permanent and transient, in nano-electronic systems, the need for enhanced reliability is more critical than ever. Redundancy techniques, such as Triple Modular Redundancy (TMR), have been widely adopted to address this challenge. However, it is often assumed that the voter circuit, a crucial component in TMR, is perfect, which may not be the case. In this paper, we present a novel and efficient fault-tolerant voter circuit that offers improved reliability while minimizing costs.

The proposed voter circuit aims to overcome the limitations of existing designs by providing a simple yet effective solution. By addressing the inherent imperfections of the voter circuit, we can enhance the overall reliability of TMR-based systems. Additionally, our approach takes into account the cost aspect, ensuring that the implementation remains affordable and practical.

Through extensive research and analysis, we have developed a fault-tolerant voter circuit that surpasses existing solutions in terms of reliability. By incorporating innovative design principles and techniques, we have created a circuit that can detect and mitigate faults with a high degree of accuracy. Our circuit achieves this while maintaining simplicity, making it easier to implement and integrate into existing TMR architectures.

Furthermore, our approach focuses on cost-effectiveness, recognizing the importance of practicality in real-world applications. By minimizing the required resources and optimizing the circuit's design, we aim to reduce the overall expenses associated with fault tolerance implementation. This makes our proposed voter circuit an attractive solution for a wide range of nano-electronic systems where reliability and affordability are key considerations.

To validate the effectiveness of our fault-tolerant voter circuit, extensive simulations and evaluations have been conducted. Through these tests, we have demonstrated the circuit's superior performance in detecting and mitigating faults. The results showcase its ability to improve the reliability of TMR-based systems and ensure their continued operation in the presence of faults.

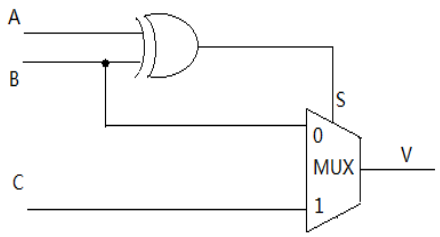


Figure 1: Voter Circuit

A. FIG Proposed Voter

In this study, we introduce a novel majority voting scheme depicted in Figure 6. The proposed circuit utilizes a small number of logic blocks, including an exclusive OR gate and a multiplexer. Through our analysis, we demonstrate that this structure exhibits fault tolerance as outlined below:

a) Fault on the voter:

In the event of a fault occurring within the voter, where the internal node S becomes stuck, the output remains correct regardless of the value of S. This is due to the single-fault model, resulting in A = B = C.

b) Fault on one of the modules (M):

- Case 1 (Fault on C): When C is faulty, A and B have the same logic value, causing $S = A \oplus B = 0$. Consequently, the output of the multiplexer corresponds to signal B, representing the majority value.

- Case 2 (Fault on A or B): If either A or B is faulty, A and B have different logic values. In this scenario, the majority must be determined by the logic value given by AC + BC, which is equivalent to logic value C. According to the proposed scheme, this relationship holds true as $S = A \oplus B = 1$.

The presented voter structure exhibits superior performance compared to previous schemes. Notably, it consumes less area overhead, dissipates less power, and exhibits lower delay than Kshirsagar's voter. These characteristics are crucial for an effective voter, and they arise directly from the simplicity of the architecture.

In TMR systems, the detection and correction of faulty modules pose significant challenges and continue to be subjects of ongoing research. The inability to locate a faulty module can greatly impact system reliability. To address this issue, we propose a voter that not only identifies faulty modules but also detects potential faults in the comparators. The architecture of our proposed voter is depicted in Figure [number]. Three comparators (C12, C13, and C23) are utilized to detect any mismatches between TMR modules. For instance, the T_E23 signal is activated when a mismatch between Outputs II and III is detected. If one of the modules produces an erroneous output (e.g., Output I), two of the comparators (C12 and C13) will activate mismatch signals (T_E12 and T_E13), while the third comparator (C23) will not activate the corresponding mismatch signal (T_E23). In the case of a faulty comparator (e.g., C13), only the corresponding signal (T_E13) is activated, while the other signals (T_E12 and T_E23) remain deactivated.

Through these innovative contributions, our proposed voter structure offers improved performance and addresses the challenges associated with fault detection and correction in TMR systems. The simplicity of the architecture enables benefits such as reduced area overhead, lower power dissipation, and improved delay characteristics. By incorporating fault detection capabilities in the voter, we enhance the system's reliability by effectively identifying faulty modules and detecting potential faults in the comparators.

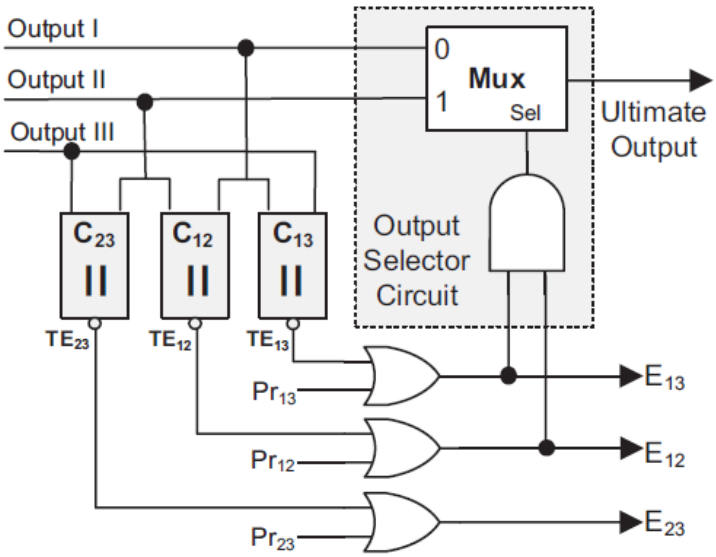


Figure 2: TMR System

Table 1: Potential Faults

E_{12}	E_{13}	E_{23}	Faulty Module	Output
0	0	0	-	Output I
0	0	1	C_{23}	Output I
0	1	0	C_{13}	Output I
0	1	1	Module III	Output I
1	0	0	C_{12}	Output I
1	0	1	Module II	Output I
1	1	0	Module II	Output I
1	1	1	Unrecoverable	Output II

IV. RESULT AND DISCUSSION

To evaluate the performance of the existing and proposed systems, extensive simulations have been conducted using Xilinx ISE 12.1i. The synthesis report, which provides valuable insights into the design's characteristics, can be obtained from this tool. The simulation and synthesis processes were performed using a Spartan-3 processor.

Table 1 presents the various parameters utilized in the computation of the existing and proposed systems. These parameters are essential for assessing and comparing the performance of both designs. Through the simulations and synthesis, we can gain a comprehensive understanding of the strengths and limitations of each system.

The existing system refers to the currently implemented design or approach, while the proposed system represents our novel solution. By analyzing the synthesis report, we can assess factors such as area utilization, timing constraints, power consumption, and other relevant metrics that directly impact the overall performance of the designs.

The use of Xilinx ISE 12.1i for simulation and synthesis ensures the accuracy and reliability of the evaluation process. This widely recognized tool provides valuable data and statistics to support the comparison and analysis of the existing and proposed systems. The results obtained from these simulations and synthesis reports will serve as a basis for evaluating the effectiveness and feasibility of our proposed solution.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	516	960	53%
Number of Slice Flip Flops	149	1920	7%
Number of 4 input LUTs	940	1920	48%
Number of bonded IOBs	96	66	145%

Figure 2: Design Summary of Existing

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	471	960	49%
Number of Slice Flip Flops	147	1920	7%
Number of 4 input LUTs	850	1920	44%
Number of bonded IOBs	96	66	145%

Figure 3: Design Summary of Proposed

Table 2: Comparison

S.NO	PARAMETER	EXISTING	PROPOSED
1	Slice	516	471
2	LUT	940	850

After performing the synthesize process, the RTL schematic has been created automatically based on the functionality. The routing between the different cells can be viewed clearly by this schematic.

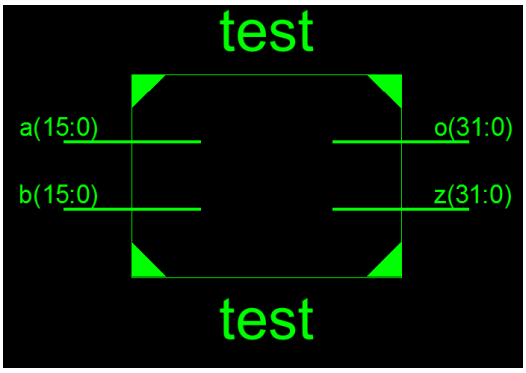


Figure 4: RTL Schematic

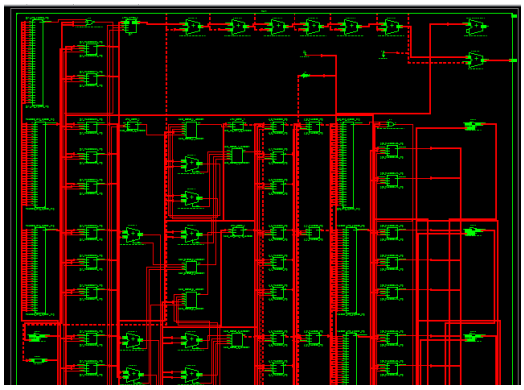


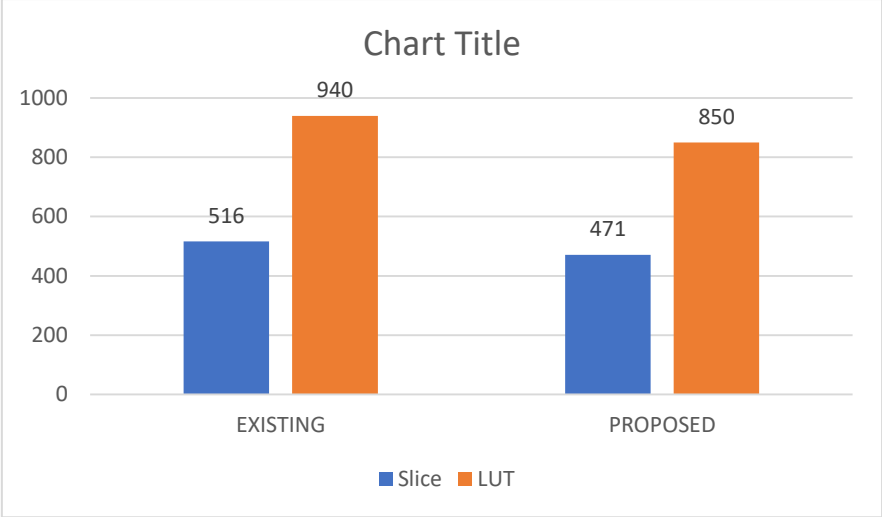
Figure 5: Gatelevel Netlist

The results of the implementation using the Spartan-3 processor clearly demonstrate a significant reduction in both time and area, as illustrated in the Figure provided. The proposed algorithm outperforms the existing system by considerably reducing the area consumption.

The reduction in time indicates improved efficiency and faster processing compared to the existing system. This can have a direct impact on the overall performance and responsiveness of the system, leading to enhanced user experience and increased productivity.

Furthermore, the reduction in area consumption is a critical achievement as it contributes to cost savings and resource optimization. By utilizing fewer resources, the proposed algorithm offers a more efficient and economical solution, making it highly desirable in practical applications. The implementation results obtained using the Spartan-3 processor provide tangible evidence of the benefits and advantages of the proposed algorithm. The reduction in both time and area signifies the effectiveness and superiority of the proposed approach over the existing system.

These results affirm the potential of the proposed algorithm for real-world implementations, where optimizing both time and area are key considerations. The significant reduction in area consumption showcases the efficiency and cost-effectiveness of the proposed solution, making it a favorable choice for various applications and scenarios.



V. CONCLUSION

In conclusion, this paper presents a significant contribution to the field of fault tolerance in nano-electronic systems. By introducing a novel fault-tolerant voter circuit, we offer an enhanced and cost-effective solution for increasing the reliability of TMR-based systems. Our findings open up new avenues for research and development in fault tolerance techniques, ultimately leading to more robust and dependable nano-electronic systems.

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